
From: [REDACTED]@oracle.com>
To: chantal dumont <chantal.dumont@oracle.com>
CC: [REDACTED]@oracle.com>
Sent: 9/23/2013 9:43:34 PM
Subject: Can we move forward with [REDACTED] at [REDACTED]

Hi Chantal,

Do you have a final decision on [REDACTED]

Thanks,
[REDACTED]

On 9/20/2013 2:51 PM, chantal dumont wrote: Hi [REDACTED]

Give me until Monday. Is the candidate in a hurry to make a decision?

Thanks,

cd

P.S. I don't usually look at these until I'm approving an offer. Please change the subject if it requires my attention.

On 9/19/2013 3:25 PM, [REDACTED] wrote:
Hi Chantal,

The manager [REDACTED] for this offer has gotten back to me.
He tells me that he can increase the offer to [REDACTED] but his management can't justify the [REDACTED] salary of [REDACTED]

The candidate's expectation is [REDACTED]

Is it okay to move forward with [REDACTED]

Thanks,
[REDACTED]

On 9/13/2013 9:41 PM, chantal dumont wrote: Hi [REDACTED]

Please make sure your staff knows the intern salary rule. Our interns are brought back at the [REDACTED] range. I returned the offer for [REDACTED] his salary was extremely low for a returning intern.

Let me know if the manager has an issue with going higher.

thanks,

Chantal

On 9/12/2013 2:02 PM, [REDACTED] wrote:

Exhibit P-334

Hi Chantal,

Forwarding approvals for [REDACTED] (UPenn).
[REDACTED] is an intern over the summer.

This is a Fowler hire.

Regards,
[REDACTED]

----- Original Message -----

Subject: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn

Date: Thu, 12 Sep 2013 22:10:22 +0200

From: [REDACTED]

To: [REDACTED]

CC: [REDACTED]

Approved
[REDACTED]

On Sep 12, 2013, at 6:45, [REDACTED]@oracle.com> wrote:

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,
[REDACTED]

----- Original Message -----

Subject: Fwd: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn

Date: Wed, 11 Sep 2013 10:00:53 -0700

From: [REDACTED]

Organization: Oracle Corporation

To: [REDACTED]@oracle.com

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,
[REDACTED]

----- Original Message -----

Subject: Fwd: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn

Date: Mon, 09 Sep 2013 16:09:58 -0700

From: [REDACTED]

Organization: Oracle Corporation

To: [REDACTED]@oracle.com
CC: [REDACTED]

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,
[REDACTED]

----- Original Message -----

Subject: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn
Date: Mon, 9 Sep 2013 16:05:43 -0700 (PDT)
From: [REDACTED]
To: [REDACTED]

Approved.

Thanks,
[REDACTED]

Vice President
Engineering & Compute Tools
Oracle Microelectronics
[REDACTED]

From: [REDACTED]
Sent: Monday, September 09, 2013 2:37 PM
To: [REDACTED]
Cc: [REDACTED]
Subject: Fwd: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,
[REDACTED]

----- Original Message -----

Subject: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn
Date: Mon, 09 Sep 2013 14:31:15 -0700
From: [REDACTED]
Organization: Oracle Corporation
To: [REDACTED]
CC: [REDACTED]

Approved.
[REDACTED]

On 9/9/2013 2:13 PM, [REDACTED] wrote:

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,
[REDACTED]

----- Original Message -----

Subject:Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [REDACTED] of UPenn

Date:Mon, 09 Sep 2013 14:09:29 -0700

From:[REDACTED]

Organization:Oracle Corporation

To:[REDACTED]

Approved.

More information about the candidate:

[REDACTED] will be hired as an IC2 and will join the [REDACTED] analysis team to will work on the development of new applications for [REDACTED] analysis and verification for our [REDACTED] processors. As the industry trends toward more improvements and optimization at the [REDACTED] level, our team need more help in this area.

[REDACTED] is currently working on his master degree in Electrical Engineering at the University of Pennsylvania. He is expected to graduate in May 2014 and will be available to work in June 2014. [REDACTED] completed his Bachelor degree in Electrical Engineering from Zhejiang University, among the top schools in China, with 3.82 GPA.

During this summer of 2013, [REDACTED] completed a 14 weeks internship program in Oracle Microelectronics as part of our [REDACTED] development team. [REDACTED] have learned about our domain, our development environment, our tools and challenges. He performed very during his internship where he developed C++ code, design new software components, and built new regressions for our tools. We felt very positive about his performance. He learned very fast and was able to complete his assigned tasks on schedule.

[REDACTED] did courses in circuit design and Electronics Design Automation, and did various projects in hardware design and software engineering which meets our requirements. For the remaining two semesters in his MS degree, [REDACTED] will be taking courses that are relevant to our domain and further improve his skills for RTL application development.

Thanks,
[REDACTED]

On 9/9/2013 1:52 PM, [REDACTED] wrote:

Hi [REDACTED]

Please approve the following offer and return to me as soon as possible.

Thanks,

Candidate: [REDACTED]
Title: Hardware Engineer (100320)
Group Name: Processor Design Tools Group (SN58)
Hiring Manager: [REDACTED]
Salary: [REDACTED]
Relocation: Silver Level for College Hires
Sign-on Bonus [REDACTED]
Stock: [REDACTED]
Intended start date: July 2014

RESUME:

EDUCATIONAL BACKGROUND

University of Pennsylvania, Sep.2012 - Expected May.2014

School of Electrical and Engineering: M.S.E in EE, Current GPA: 3.95/4

Zhejiang University, Sep.2009 - June 2012

School of Electrical and Engineering: Bachelor in EE, GPA: 3.82/4

RELATED GRAD-LEVEL COURSES

Digital Integrated Circuit and VLSI, Analog Integrated Circuit, RF Integrated Circuit, Electronic Design Automation, Analysis of Algorithms, Database & Info Systems, Computer Architecture, Digital Signal Processing, Network & Protocols

INTERNSHIP

2013 hardware summer intern at Oracle Corporation, [REDACTED] group.

Use Sun Ray client and develop in CAD and TAHOE environment.

Develop and check in C++ code to SVN trunk for RTL development group involving two projects.

Fix bugs in the exiting scripts and source code at Register-transfer level.

Build up regression test and EZT for the new tool.

JOURNAL LIST & PATENTS

[REDACTED] "Alternative Formulation for Unit Commitment", Power Engineering and Automation International Conference (PEAM 2012)

Patents:

- o "A Smart Elevator with Higher Security"

- o "Automatic Up-and-Down Microphone Holder"

PROJECTS & RESEARCH EXPERIENCE

VLSI 8-bit ALU Design

Design schematic in Cadence for 12 functional components in ALU.

Write Verilog HDL to verify functionality.

Do full chip layout using Cadence Virtuoso and run DRC and LVS.

Do retiming to shorten the critical path and increase operation speed.

EDA power-aware design on partially defective FPGA

Develop tools to match, cluster, and place a circuit netlist onto a partially defective FPGA.

Implement Simulated-Annealing and write out the placement C code based on t-vpack/vpr package.

Use ACE2.0 to generate transition probability and calculate dynamic power dissipation.

Build new power-aware model and tune parameters to achieve the SRS.

Digital Frequency Meter Design Using FPGA

Use Verilog HDL and block diagram to design and code digital frequency meter.

Run simulation on Quartus2 and download the code to Xilinx FPGA.

Recode with VHDL and compare the difference between VHDL and Verilog HDL.

Fully Differential Op-Amp Design

Design the schematic and test bench of a fully differential Op-Amp with Specs.

Modify the parameters of Nmos/Pmos transistors and triple the gain.

WiFi Indoor Positioning System

Build a Client-Server model based on IP/TCP protocol and socket programming; create database.

Apply Fingerprint algorithm and Naive Bayesian algorithm to develop an Android App positioning.

Filter Channel Decomposition and Adaptive Filter Design

Use Matlab to design and implement 4-Channel reconstruction filter-bank.

FIR adaptive filter design on Adaptive Interference Cancellation and Adaptive Equalization.

Conduct research in Professor Quanyuan Jiang's group of Power System Optimization and algorithm, responsible for Power Optimization using Mixed-integer Linear Programming algorithm.

HONORS & AWARDS

Excellent Student Awards Zhejiang Univ., 2010-2012

Second-Class Scholarship for Outstanding Merits Zhejiang Univ., 2009-2012

Third-Class Mathematics Modeling Competition of Zhejiang Univ., 2011

Fifth National Teenager Innovation Prize, 2009

First-Class Prize of National Teenager Math Competition (rank 4th), 2008

QUALIFICATIONS

Programming Language: C++, C, Java, Python

Scripting Language: Perl, Python

HDL: Verilog, System Verilog, VHDL, block diagram

OS: Linux, Unix, Solaris, Windows

Proficient user of: gdb, Cadence, ADS, Matlab, Quartus, Sonnet, Multisim, OrCAD, Visual Studio

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[REDACTED] Senior Hardware Manager

Phone: [REDACTED]

Oracle [REDACTED] Group

Oracle is committed to developing practices and products that help protect the environment

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[REDACTED]
Recruiting Specialist
Oracle College Recruiting
[REDACTED]

Recruiting Specialist
Oracle College Recruiting