From: Les Cundall <les.cundall@oracle.com>
To: Elizabeth Lee <liz.lee@oracle.com>
Sent: 3/14/2014 1:01:45 AM
Subject: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted]

Sorry...didn't recall...Les

On 3/13/2014 5:50 PM, Elizabeth Lee wrote:
I forwarded my email discussion with Chantal. She suggested higher due to previous work exp.

Liz

Sent from my iPhone

On Mar 13, 2014, at 5:37 PM, Les Cundall <les.cundall@oracle.com> wrote:

No Ph.D, correct? How did you arrive at the proposed salary?

-------- Original Message --------
Subject: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted]
Date: Thu, 13 Mar 2014 17:30:44 -0700
From: Les Cundall
Organization: Oracle Corporation
To:liz lee

Why only $[redacted]?

On 3/13/2014 2:16 PM, liz lee wrote:
Fowler

-------- Original Message --------
Subject: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted]
Date: Wed, 12 Mar 2014 19:37:29 -0400
From: Bill Nesheim
To:liz lee
CC: Neal Pollack , David Chieu , andy.roach@oracle.com

Approved.
-- Bill

Bill Nesheim | Vice President | Oracle Solaris Platform Engineering
Office: +16038973775 / Cell: +16035530251
1 Oracle Drive, Nashua NH 03062

On Mar 12, 2014, at 7:22 PM, liz lee <liz.lee@oracle.com> wrote:

Exhibit P-183

Hi Bill,

Please approve the following offer and return to me as soon as possible.

Thank you,

Liz
On 3/12/2014 4:17 PM, Neal Pollack wrote:
APPROVED.

Neal Pollack

On 3/12/2014 4:12 PM, liz lee wrote:
Hi Neal,

Please approve the following offer and return to me as soon as possible.

Thank you,

Liz
On 3/12/2014 4:08 PM, David Chieu wrote:
Approved.

-- David Chieu

On 3/12/2014 3:35 PM, liz lee wrote:
Hi David,

Please approve the following offer and return to me as soon as possible.

Thank you,

Liz

Candidate: [redacted]
Title: Software Engineer (10520)
Group: x64 Platform SW Engineering (AV22)
Hiring Manager: David Chieu
Salary: $[redacted]
Relocation: Silver Level for College Hires
Sign-on Bonus: $[redacted]
Stock: As approved by Larry Lynn
Intended start date: March 2014

RESUME:

[redacted]
e-mail: [redacted]@cornell.edu
cell: 785-312-2818

Education
Cornell University Ithaca, NY
PhD candidate, College of Electrical and Computer Engineering,
Olin Fellowship, August 2012-May 2013

Massachusetts Institute of Technology; Cambridge, MA
Masters of Engineering in Electrical Engineering, September 2009
GPA: 4.6/5.0
Concentration: Devices, Circuits & Systems

Bachelor of Science in Electrical Engineering, June 2008;
GPA: 4.3/5.0

Lawrence High School; Lawrence, KS
National Merit Scholar; Valedictorian, June 2004;
GPA: 4.0/4.0

Leadership experience:
Raytheon's Engineering Leadership Development Program (RELDP), Class of 2012
selected for Raytheon's corporate program with senior leadership mentoring to develop technical leadership

Department of Defense Secret Clearance; Six Sigma Specialist
Title: Engineer II-Senior Engineer I, 2009-2012

Engineer Week 2010 at Raytheon, Planning Committee
Society of Women Engineers: Treasurer ('10) & Publicity Committee Chair ('09), Planning committee for 2009 Northeast regional SWE conference

Work Experience:
Raytheon, Network Centric Systems; North Dallas, Tx
Experience Software/Systems Radar Integration, (November 2011-August 2012)
Responsible for component radar integration on a Ku-band radar product. Tasks include integrating and executing embedded software in a ground radar product.
Raytheon, Integrated Defense Systems; Andover, MA

Semiconductor Process Engineer, (March 2011-November 2011)
Worked in clean-clean room facility. Responsible for various process improvement and failure analysis in the fabrication of microwave GaN power amplifier.
Process improvement to SiN passivation on AlGaN/GaN HEMTs: investigating effects of thin film characteristics and stress on film to improve electric breakdown and reliability
Optimizing ohmic contacts on AlGaN/GaN HEMTs: specifically improving surface morphology and electric contact
. RF/DC Failure analysis: Confocal imaging, light emission to understand device reliability and fabrication irregularities.

Raytheon, Network Centric Systems; Fort Wayne, IN
Hardware Engineer, (July 2009-March 2011)
VHDL code and test integration to support a built-in self-test capability in wideband software-defined radios. Test capability checks the operation of transmit and receive paths of the radio by comparisons of 3 detector values in the RF/RE circuit.
Also designed testbench and simulation to analyze expansion of channel capacity and encoding/decoding for multiple-input multiple output (MIMO) software defined radios

MIT Microsystems Technology Laboratories; Cambridge, MA
Graduate Research Assistant, (Jun. 2008-July 2009)
Advisor: Professor A. Akinwande

Research focus: Designing, fabricating and characterizing of high aspect ratio silicon pillars with ohmic contacts as test structures for the un-gated FET. The test structure was constructed (1) to provide accurate and precise characterization of a single un-gated FET device; (2) demonstrate high saturation current (1 mA) capability; (3) investigate the effects on key device parameters when connecting different-sized array of pillars in parallel.

Undergraduate Research Assistant, (Feb. 2007-Jun. 2008)
Advisor: Professor A. Akinwande
Research focus: understanding and modeling device behavior of a proposed un-gated FET device fabricated by vertical high-aspect ratio (~1 x 1 µm x 100µm) silicon pillars that exhibits current-limiting behavior. Efforts include (1) developing analytical models to accurately describe device behavior; (2) simulating single transistor behavior to verify device operation. (3) extracting key device parameters for device analysis. (4) characterizing the prototype device fabricated by Principal Research Scientist, Dr. L. Velasquez.

University of Kansas, Information and Telecommunication Technology Center; Lawrence, KS
Summer Research Assistant, (June-August 2006)
Mentor: Professor Victor Frost
Research focus: Applied statistical methods of hypothesis and likelihood ratio testing to detect route change in communication networks. Verified results through simulations to detect borders of two distinct sets of random gamma distributed data.

NSF Research Experience for Undergraduates (REU), (June-August 2005)
Mentor: Professor Victor Frost
Research focus: Explored use of discrete packet simulation in place of fluid network simulation to model fractional Brownian motion in communication networks.

List of Publications:
Y. Niu, D. Mussmann, "FPGA based Waveform PHY Architecture for MIMO in a Two-Channel Software Defined Radio System," Raytheon Symposium Information Systems and Computing Technology network (ISaCTN), June 2011.
Y. Niu, D. Mussmann, "Hardware-in-the-Loop Design Verification Testing for Software-Defined Radio Waveforms," Software Defined Radio Wireless Innovation Forum, Dec 2010.
Y. Niu, A.I. Akinwande, "Current limiters based on silicon pillar un-gated FET for Field Emission application," Master of Engineering Thesis, Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, July 2009.
L.F. Velasquez-Garcia, Y. Niu, and A.I. Akinwande, "Advanced Cathodes for Novel Sub mm-Wave Compact Sources," Government Microcircuit Application & Critical Technology Conference, March 2009.
Y. Niu, L.F. Velasquez-Garcia, A.I. Akinwande, "Uniform High Current Field Emission of Electrons from Si and CNF FEAs individually controlled by Si Pillar Ungated FETs," Microsystems Annual Research Conference, Jan 2009
L.F. Velasquez-Garcia, Y. Niu, and A.I. Akinwande, "Fabrication of Nanosharp High-Aspect-Ratio Probes for Biomedical Sensing" MTL Workshop on Next-Generation Medical Electronic Systems, Dec. 4-5 2008.
L.F. Velasquez-Garcia, B. Adeoti, Y. Niu, and A.I. Akinwande, "Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually controlled by Si Pillar Ungated FETs," IEEE International Electron Devices Meeting, 2007, pp. 599-602.

Relevant Courses:
Microelectronics, Circuits and Devices (major concentration):
Integrated Microelectronics Devices (6.720), Nanoelectronics (6.719), Microelectronics Processing Technology (6.152J), Microelectronic Devices and Circuits (6.012), Circuits and Electronics (6.002)
Electromagnetics (minor concentration):
Electromagnetic Fields, Forces & Motion (6.641), Electromagnetics (6.013), Modern Optics Lab (6.161), Physics II: Electricity & Magnetism (8.02),
Signal Processing and Communications (minor concentration):
Digital Image Processing (6.344), Communication, Control, and Signal Processing (6.011), Signals and Systems (6.003)

Mathematics and Computer Science:
Computation Structures (6.004), Mathematics for Computer Science (6.042), Artificial Intelligence (6.034), Structure and Interpretation of Computer Programs (6.001), Probabilistic Systems Analysis & Applied Probability (6.041), Differential Equations (18.03), Linear Algebra (18.06), Partial Differential Equations (18.303).

Languages:
Fluent in English; Conversational German and (Mandarin) Chinese

Interests:
MathMovesU Ambassadors—taking MMU program into area schools (2011). Three Rivers Ping Pong club (2010-2011); Volunteer for Rube-Goldberg Middle School Project(2010); Volunteer for Study Connections (2009-2011); Piano; Pencil Sketching; Badminton MIT Club (2008-2009); Ping Pong MIT Club (2006-2009); Volleyball MIT Club (2004-2008)

Master's Thesis Abstract:
This research investigates the use of vertical silicon un-gated field effect transistors (FETs) as current limiters to individually ballast field emitter arrays and provide a simple solution to three problems that have plagued field emission arrays—emission current uniformity, emission current stability and reliability. The un-gated FET consists of high aspect ratio silicon pillars individually connected in series with silicon or carbon nanofiber (CNF) emission tips. The transistors were designed as high aspect ratio silicon

pillars in order to achieve velocity saturation of carriers and obtain current source-like characteristics. Device and process simulations were initially conducted using SILVACO software to solidify the derived analytical model and optimize design parameters. Devices were fabricated and characterized in the Microsystems Technology Laboratory. The main outcome of this study is that individual control of field emitter current is feasible using un-gated FETs

based vertical Si pillars.

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Neal Pollack | Senior Manager, Engineering Site Leader
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