From: chantal dumont
To: duhong trinh
CC: Les.cundall@oracle.com; Milton Liu
Sent: 9/14/2013 4:41:14 AM
Subject: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted] of UPenn

Hi Milton,

Please make sure your staff knows the intern salary rule. Our interns are brought back at the [redacted] of the range. I returned the offer for [redacted] as his salary was extremely low for a returning intern.

Let me know if the manager has an issue with going higher.

thanks,

Chantal

On 9/12/2013 2:02 PM, duhong trinh wrote:
> Hi Chantal,
>
> Forwarding approvals for [redacted] (UPenn).
> [redacted] was an intern over the summer.
>
> This is a Fowler hire.
>
> Regards,
> Hong
>
>
> -------- Original Message --------
> Subject: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted]
> of UPenn
> Date: Thu, 12 Sep 2013 22:10:22 +0200
> From: Mike Splain <mike.splain@oracle.com>
> To: Hong Trinh <duhong.trinh@oracle.com>
> CC: Mohammed Jamil <jamil.mohd@oracle.com>
>
>
>
> Approved
>
> Mike
>
> On Sep 12, 2013, at 6:45, Hong Trinh <duhong.trinh@oracle.com
> <mailto:duhong.trinh@oracle.com>> wrote:
>
>> Hi Mike,
>>
>>
>> Please approve the following offer and return to me as soon as possible.
>>
>> Thanks,
>> Hong
>>
>> -------- Original Message --------
>> Subject: Fwd: Fwd: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL
>> REQUEST FOR [redacted] of UPenn
>> Date: Wed, 11 Sep 2013 10:00:53 -0700
>> From: Hong Trinh <duhong.trinh@oracle.com>
>> Organization: Oracle Corporation
>> To: mike.splain@oracle.com
>>
>>

Exhibit P-182

>>
>> Hi Mike,
>>
>>
>> Please approve the following offer and return to me as soon as possible.
>>
>> Thanks,
>> Hong
>>
>> -------- Original Message --------
>> Subject: Fwd: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST
>> FOR [redacted] of UPenn
>> Date: Mon, 09 Sep 2013 16:09:58 -0700
>> From: duhong trinh <duhong.trinh@oracle.com>
>> Organization: Oracle Corporation
>> To: mike.splain@oracle.com
>> CC: Mohammed Jamil <jamil.mohd@oracle.com>
>>
>>
>>
>> Hi Mike,
>>
>>
>> Please approve the following offer and return to me as soon as possible.
>>
>> Thanks,
>> Hong
>>
>>
>> -------- Original Message --------
>> Subject: RE: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR
>> [redacted] of UPenn
>> Date: Mon, 9 Sep 2013 16:05:43 -0700 (PDT)
>> From: Rob Mains <rob.mains@oracle.com>
>> To: Hong Trinh <duhong.trinh@oracle.com>
>>
>>
>>
>> Approved.
>>
>> Thanks,
>>
>> Rob
>>
>> Vice President
>>
>> Engineering & Compute Tools
>>
>> Oracle Microelectronics
>>
>> 408.607.4879
>>
>> *From:*duhong trinh
>> *Sent:* Monday, September 09, 2013 2:37 PM
>> *To:* Rob Mains
>> *Cc:* Mohammed Jamil
>> *Subject:* Fwd: Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR
>> [redacted] of UPenn
>>
>> Hi Rob,
>>
>>
>> Please approve the following offer and return to me as soon as possible.
>>
>> Thanks,
>> Hong
>>
>> -------- Original Message --------

>>
>> *Subject: *
>>
>>
>>
>> Re: Fwd: Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted]
>> of UPenn
>>
>> *Date: *
>>
>>
>>
>> Mon, 09 Sep 2013 14:31:15 -0700
>>
>> *From: *
>>
>>
>>
>> Michel Laudes <michel.laudes@oracle.com>
>> <mailto:michel.laudes@oracle.com>
>>
>> *Organization: *
>>
>>
>>
>> Oracle Corporation
>>
>> *To: *
>>
>>
>>
>> duhong trinh <duhong.trinh@oracle.com> <mailto:duhong.trinh@oracle.com>
>>
>> *CC: *
>>
>>
>>
>> Mohammed Jamil <jamil.mohd@oracle.com> <mailto:jamil.mohd@oracle.com>
>>
>>
>>
>> Approved.
>>
>> Michel
>>
>> On 9/9/2013 2:13 PM, duhong trinh wrote:
>>
>> Hi Michel,
>>
>> Please approve the following offer and return to me as soon as
>> possible.
>>
>> Thanks,
>> Hong
>>
>>
>>
>> -------- Original Message --------
>>
>> *Subject: *
>>
>>
>>
>> Re: +++UNIVERSITY OFFER APPROVAL REQUEST FOR [redacted] of UPenn
>>
>> *Date: *
>>
>>

>>
>> Mon, 09 Sep 2013 14:09:29 -0700
>>
>> *From: *
>>
>>
>>
>> Mohammed Jamil <jamil.mohd@oracle.com> <mailto:jamil.mohd@oracle.com>
>>
>> *Organization: *
>>
>>
>>
>> Oracle Corporation
>>
>> *To: *
>>
>>
>>
>> duhong trinh <duhong.trinh@oracle.com>
>> <mailto:duhong.trinh@oracle.com>
>>
>>
>>
>>
>>
>> Approved.
>>
>> More information about the candidate:
>>
>> [redacted] will be hired as an IC2 and will join the RTL and Power
>> analysis team to will work on the
>> development of new applications for RTL analysis and verification
>> for our SPARC processors.
>> As the industry trends toward more improvements and optimization
>> at the RTL level, our team
>> need more help in this area.
>>
>> [redacted] is currently working on his master degree in
>> Electrical Engineering at the
>> University of Pennsylvania. He is expected to graduate in May
>> 2014 and will be available
>> to work in June 2014. [redacted] completed his Bachelor degree in
>> Electrical Engineering from
>> Zhejiang University, among the top schools in China, with 3.82 GPA.
>>
>> During this summer of 2013, [redacted] completed a 14 weeks internship
>> program in Oracle
>> Microelectronics as part of our RTL development team. [redacted] have
>> learned about our
>> domain, our development environment, our tools and challenges. He
>> performed very during
>> his internship where he developed C++ code, design new software
>> components, and built new
>> regressions for our tools. We felt very positive about his
>> performance. He learned very fast
>> and was able to complete his assigned tasks on schedule.
>>
>> [redacted] did courses in circuit design and Electronics Design
>> Automation, and did various projects
>> in hardware design and software engineering which meets our
>> requirements. For the remaining
>> two semesters in his MS degree, [redacted] will be taking courses that
>> are relevant to our domain and
>> further improve his skills for RTL application development.
>>
>> Thanks,
>> Mohammed

>>
>> On 9/9/2013 1:52 PM, duhong trinh wrote:
>>
>> Hi Mohammed,
>>
>> Please approve the following offer and return to me as soon
>> as possible.
>>
>> Thanks,
>> Hong
>>
>>
>> Candidate:[redacted]
>> Title: Hardware Engineer (100320)
>> Group Name: Processor Design Tools Group (SN58)
>> Hiring Manager: Mohammed Jamil
>> Salary:[redacted]
>> Relocation: Silver Level for College Hires
>> Sign-on Bonus:[redacted]
>> Stock: As approved by Larry Lynn
>> Intended start date: July 2014
>>
>>
>> RESUME:
>>[redacted]
>>[redacted]
>> EDUCATIONAL BACKGROUND
>>
>> University of Pennsylvania, Sep.2012 - Expected May.2014
>>
>> ·School of Electrical and Engineering: M.S.E in EE, Current
>> GPA: 3.95/4
>>
>> Zhejiang University, Sep.2009 - June 2012
>>
>> ·School of Electrical and Engineering: Bachelor in EE, GPA:
>> 3.82/4
>>
>> RELATED GRAD-LEVEL COURSES
>>
>> Digital Integrated Circuit and VLSI, Analog Integrated
>> Circuit, RF Integrated Circuit, Electronic Design Automation,
>> Analysis of Algorithms, Database & Info Systems, Computer
>> Architecture, Digital Signal Processing, Network & Protocols
>>
>> INTERNSHIP
>>
>> 2013 hardware summer intern at Oracle Corporation, Processor
>> Design Tools group.
>>
>> ·Use Sun Ray client and develop in CAD and TAHOE environment.
>>
>> ·Develop and check in C++ code to SVN trunk for RTL
>> development group involving two projects.
>>
>> ·Fix bugs in the exiting scripts and source code at
>> Register-transfer level.
>>
>> ·Build up regression test and EZT for the new tool.
>>
>> JOURNAL LIST & PATENTS
>>
>> ·Xitan Qiang, Boran Zhou, Quanyuan Jiang, "Alternative
>> Formulation for Unit Commitment", Power Engineering and
>> Automation International Conference (PEAM 2012)
>>
>> ·Patents:

>>
>> o"A Smart Elevator with Higher Security"
>>
>> o"Automatic Up-and-Down Microphone Holder"
>>
>> PROJECTS & RESEARCH EXPERIENCE
>>
>> VLSI 8-bit ALU Design
>>
>> ·Design schematic in Cadence for 12 functional components in ALU.
>>
>> ·Write Verilog HDL to verify functionality.
>>
>> ·Do full chip layout using Cadence Virtuoso and run DRC and LVS.
>>
>> ·Do retiming to shorten the critical path and increase
>> operation speed.
>>
>> EDA power-aware design on partially defective FPGA
>>
>> ·Develop tools to match, cluster, and place a circuit netlist
>> onto a partially defective FPGA.
>>
>> ·Implement Simulated-Annealing and write out the placement C
>> code based on t-vpack/vpr package.
>>
>> ·Use ACE2.0 to generate transition probability and calculate
>> dynamic power dissipation.
>>
>> ·Build new power-aware model and tune parameters to achieve
>> the SRS.
>>
>> Digital Frequency Meter Design Using FPGA
>>
>> ·Use Verilog HDL and block diagram to design and code digital
>> frequency meter.
>>
>> ·Run simulation on Quartus2 and download the code to Xilinx FPGA.
>>
>> ·Recode with VHDL and compare the difference between VHDL and
>> Verilog HDL.
>>
>> Fully Differential Op-Amp Design
>>
>> ·Design the schematic and test bench of a fully differential
>> Op-Amp with Specs.
>>
>> ·Modify the parameters of Nmos/Pmos transistors and triple
>> the gain.
>>
>> WiFi Indoor Positioning System
>>
>> ·Build a Client-Server model based on IP/TCP protocol and
>> socket programming; create database.
>>
>> ·Apply Fingerprint algorithm and Naive Bayesian algorithm to
>> develop an Android App positioning.
>>
>> Filter Channel Decomposition and Adaptive Filter Design
>>
>> ·Use Matlab to design and implement 4-Channel reconstruction
>> filter-bank.
>>
>> ·FIR adaptive filter design on Adaptive Interference
>> Cancellation and Adaptive Equalization.
>>
>> Conduct research in Professor Quanyuan Jiang's group of Power
>> System Optimization and algorithm, responsible for Power

>> Optimization using Mixed-integer Linear Programming algorithm.
>>
>> HONORS & AWARDS
>>
>> ·Excellent Student Awards Zhejiang Univ., 2010-2012
>>
>> ·Second-Class Scholarship for Outstanding Merits Zhejiang
>> Univ., 2009-2012
>>
>> ·Third-Class Mathematics Modeling Competition of Zhejiang
>> Univ., 2011
>>
>> ·Fifth National Teenager Innovation Prize, 2009
>>
>> ·First-Class Prize of National Teenager Math Competition
>> (rank 4th), 2008
>>
>> QUALIFICATIONS
>>
>> ·Programming Language: C++, C, Java, Python
>>
>> ·Scripting Language: Perl, Python
>>
>> ·HDL: Verilog, System Verilog, VHDL, block diagram
>>
>> ·OS: Linux, Unix, Solaris, Windows
>>
>> ·Proficient user of: gdb, Cadence, ADS, Matlab, Quartus,
>> Sonnet, Multisim, OrCAD, Visual Studio
>>
>> --
>> <mime-attachment.gif> <http://www.oracle.com>
>> Mohammed Jamil | Senior Hardware Manager
>> Phone: +1 4082766144 <tel:+1%204082766144> | Fax: +1 4082766144
>> <fax:+1%204082766144>
>> OracleProcessor Tools Group
>>
>> <mime-attachment.gif> <http://www.oracle.com/commitment>Oracle is
>> committed to developing practices and products that help protect
>> the environment
>>
>>
>>
>>
>
>