[redacted]

[redacted]

[redacted]@[redacted]
mobile: ([redacted]) [redacted]

Skills Summary

- Extensive experience developing software and leading software projects/teams.
- Strong expertise with java server side, compilers, debuggers, JVMs.
- Strong knowledge of Java, C and C++ programming.
- Proficient with SQL, PL/SQL, JDBC and Oracle database programming.

Professional Experience

R&D Manager, Staff R&D Engineer — **Jan 2006 – Present**
Synopsys, Inc. — **Mountain View, CA**

Development Lead for the debugger for the VCS Hardware Description Language (SystemVerilog/VHDL) digital logic simulator. The software was developed using C and C++.

- Lead (hands on) on several projects which resulted in new features and improvements in memory footprint, performance and quality of the debug infrastructure in VCS.
- Managed a team in Synopsys' India development Center.

Principal Member of Technical Staff — **May 2003 – Jan 2006**
Oracle Corporation — **Redwood Shores, CA**

Development Lead on the Job System server side component within the Oracle Enterprise Manager (EM) product. The Job System allows users to register work flows and submit jobs with various types of schedules to automate management of Oracle products, including the database, application server and applications. The software was developed using Java, Servlets, PL/SQL and Oracle databases.

- Lead on several projects to add new features to the Job System and improve its quality and performance.
- Projects included support for user created complex job types incorporating other job types, reporting of skipped job executions due to various conditions, prototyping of asynchronous dispatch of job steps using Oracle Advanced Queues, testing harness to allow testing of jobs with various schedules taking time into consideration.

Senior Software Engineer **Feb 2003 – May 2003**
Mentor Graphics Corporation **San Jose, CA**

Development of Assertion based Verification in the Modelsim mixed Hardware Description Language (Verilog/VHDL) digital logic simulator at Mentor Graphics.

Senior Software Engineer **Jan 2001 – Jan 2003**
Chameleon Systems, Inc. **San Jose, CA**

Development Lead for a compiler for a proprietary programming language (*Fabulas*) for Chameleon Systems' Reconfigurable Communications Processor (RCP). The compiler parsed *Fabulas* source code and synthesized a structural netlist that was mapped to the processor. It also produced a cycle accurate C++ simulation model for pre-mapping verification and performance tuning. The compiler was implemented in Java. The lexer and parser were implemented using ANTLR.

- Defined the syntax and semantics of the language, added language features to expose the power of the RCP and to make programming it easier.
- Designed and implemented the compiler and APIs to allow the compiler to communicate with other tools in the design flow, Mathworks' Simulink and Chameleon's Place and Route.

Member of Technical Staff **Dec 1997 - Jan 2001**
Sun Microsystems, Inc. **Palo Alto, CA**

Developer on the HotSpot Java Virtual Machine (JVM) team for the Solaris/SPARC platform. The development was done in C++ on Solaris.

- Substantial work in implementing a new fast dynamic Just In Time (JIT) compiler in the HotSpot client VM for the SPARC processor. Took the project from start to a stage where the client VM was able to run SpecJVM and some longer applications in compiled mode.
- Improving the stability and reliability of the interpreter and runtime systems for the HotSpot server VM on large server side programs and benchmarks.

Software Engineer **Feb 1995 - Dec 1997**
IKOS Systems, Inc. (acquired by Mentor Graphics) **Cupertino, CA**

Developer on a small team that developed a new high performance, native code VHDL compiler for Sun SPARC and HP PA platforms using C++ for IKOS's digital logic simulator. Individual accomplishments include the design, implementation and testing of major modules in the compiler front end (Intermediate Representation generation) and language debugger.

Education

Master of Science (MS) in Computer Science **Aug 1992 - Jan 1995**
University of Illinois at Urbana-Champaign, Illinois

Bachelor of Engineering (BE) in Computer Science **Aug 1988 - July 1992**
Birla Institute of Technology and Science, Pilani, India